

Fig. 1

(Prior Art)

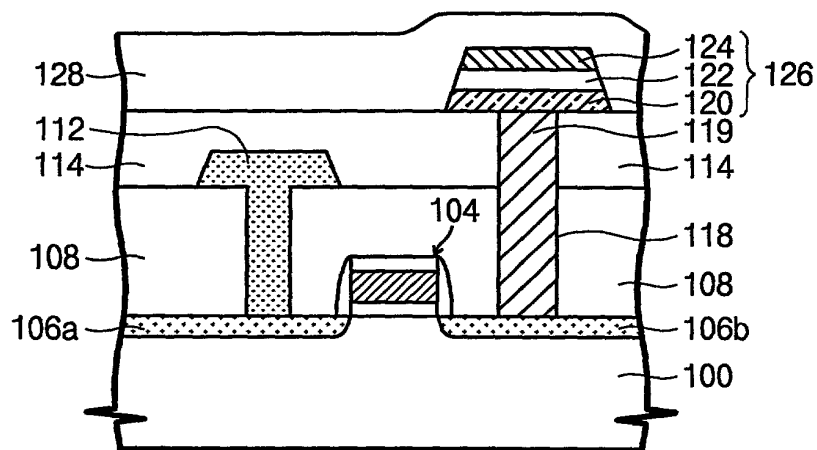


Fig. 2

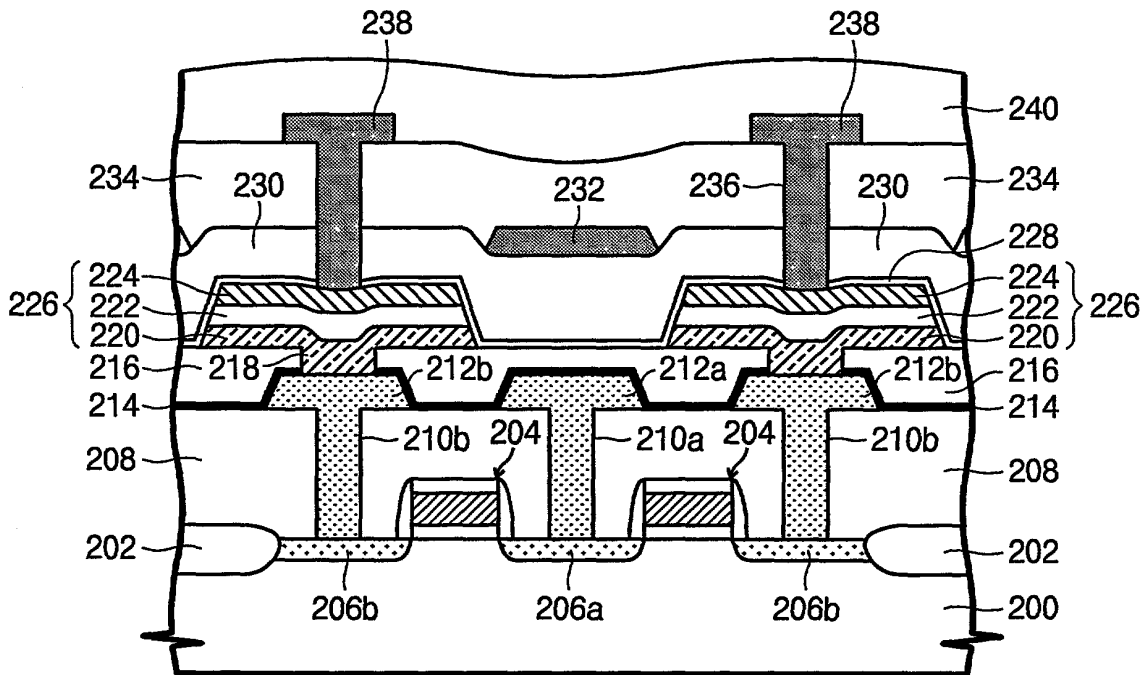


Fig. 3A

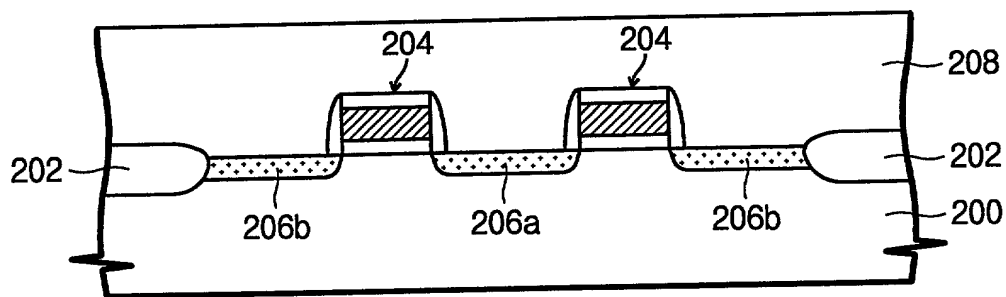
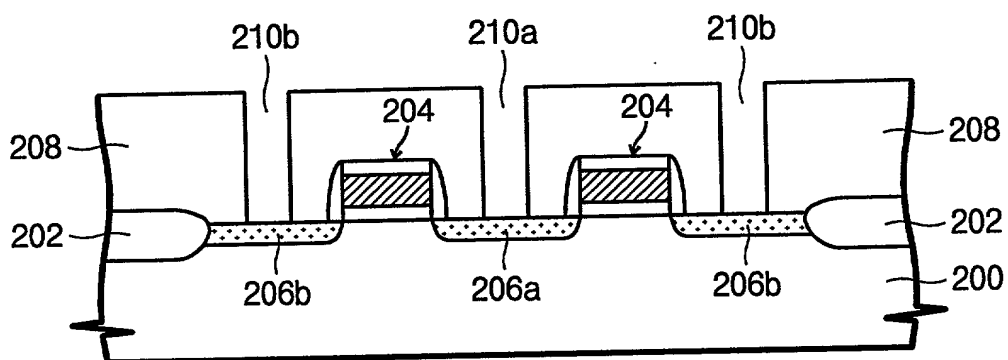


Fig. 3B



A cross-sectional view of a semiconductor device. The device features a substrate 200 with a top layer 202. A series of gate electrodes 212a and 212b are formed on the top layer. Between the gate electrodes are channel regions 210a and 210b. A source/drain region 204 is located between the channel regions. The top layer 202 is doped, as indicated by the stippled pattern. The gate electrodes 212a and 212b are also doped. The channel regions 210a and 210b are undoped. The source/drain region 204 is doped. The device is connected to a power supply 208.

A cross-sectional view of a semiconductor device. The device features a substrate 200 with a trench 202. A layer 204 is formed within the trench 202. A layer 206a is formed on the bottom surface of the trench 202. A layer 206b is formed on the side walls of the trench 202. A layer 208 is formed on the top surface of the substrate 200. A layer 210a is formed on the top surface of the layer 204. A layer 210b is formed on the top surface of the layer 206b. A layer 212a is formed on the top surface of the layer 210a. A layer 212b is formed on the top surface of the layer 210b. A layer 214 is formed on the top surface of the layer 212a. A layer 216 is formed on the top surface of the layer 212b.

Fig. 3E

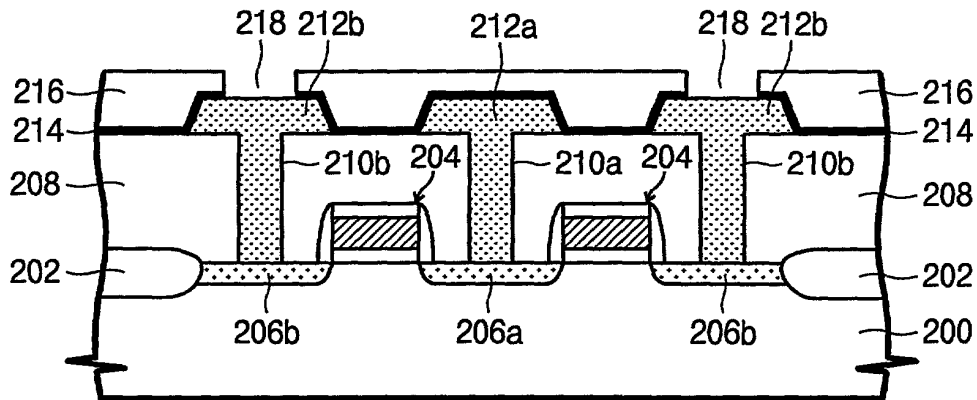


Fig. 3F

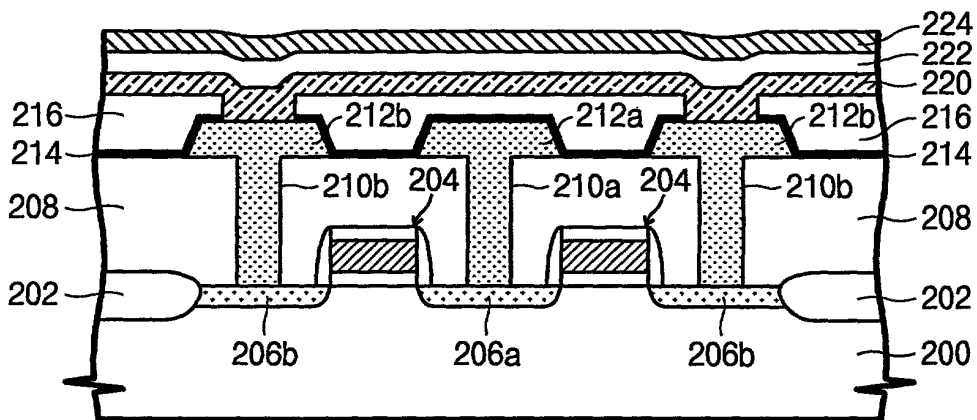


Fig. 3G

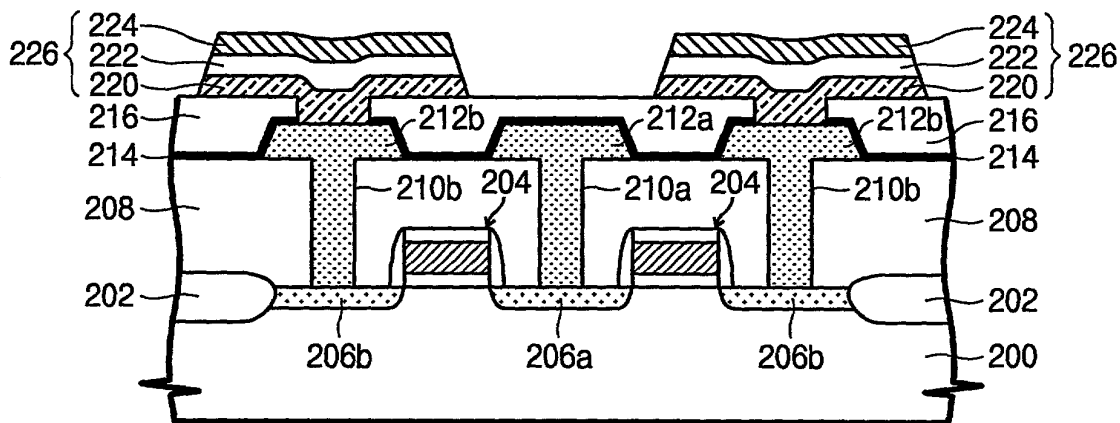


Fig. 3H

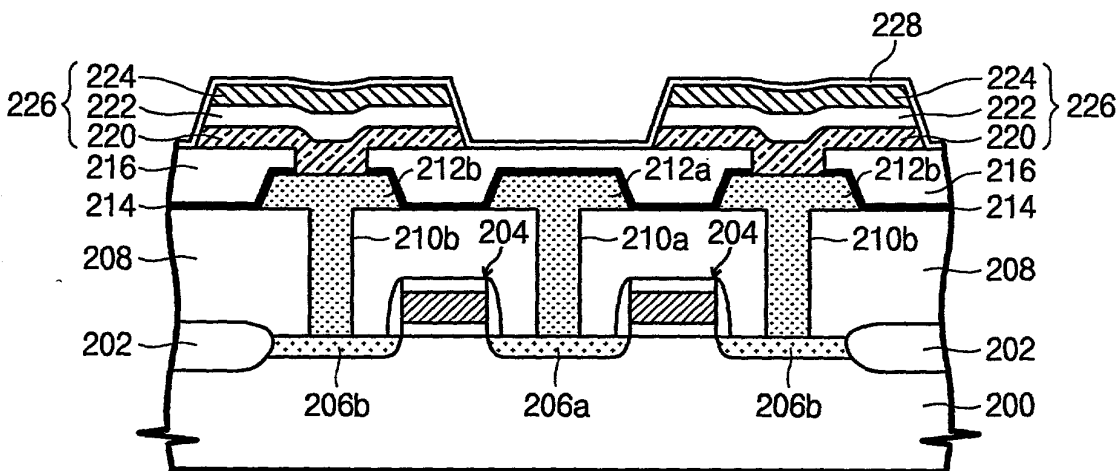


Fig. 3I

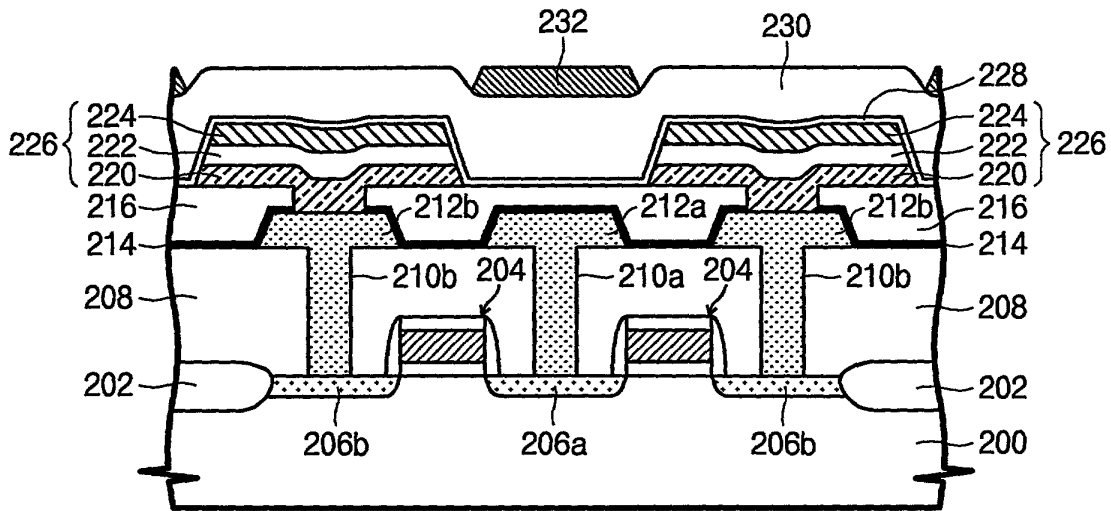


Fig. 3J

